MT6365 Product Brief

Version: 1.0

Release date: 2023-09-01

The full datasheet is available with an NDA

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Version History

Version	Date	Description
1.0	2023-09-01	Official release

Table of Contents

List of Figures

List of Tables

1 Overview

1.1 Features

- Handles smart phone baseband power management
- Input range: 2.6~5V
- 9 buck converters and 33 LDOs optimized for specific smart phone subsystems
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC
- 32K-Crystal-less RTC oscillator for system timing, 1.8 clock buffer output
- SPI interface
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Watchdog reset
- Flexibility hardware PMIC reset function
- Power-on reset and start-up timer
- Precision voltage, temperature, and current measurement fuel gauge
- Storage card plug-out protection
- 203-pin WFBGA package

1.2 Applications

- MT6365 is ideal for power management of smart phones and other portable systems.
- Industrial HMI, desktop POS, KIOSK, digital signage

1.3 General Description

MT6365 is a power management system chip optimized for handsets and smart phones, containing 9 buck converters and 33 LDOs optimized for specific smart phone subsystems.

Sophisticated controls are available for power-up and the RTC alarm. MT6365 is optimized for maximum battery life, allowing the RTC circuit to stay alive without a battery for several hours.

MT6365 adopts SPI interface and two SRCLKEN control pins to control buck converters, LDOs, and various drivers; it provides enhanced safety control and protocol for handshaking with baseband.

MT6365 is available in a 203-pin WFBGA package. The operating temperature ranges from -40°C to +85°C.

1.4 Ordering Information

Table 1-1. Ordering options

Order #	Marking	Temp. range	Package
MT6365IAW/B		-40 ~ +85°C	WFBGA 203 pins
MT6365IBW/B		-40 ~ +85°C	WFBGA 203 pins

1.5 Boot-up Voltage Table on Each Part

Table 1-2. Boot-up voltage table

BUCK name	Part number	Default voltage (V)	Default on (Y/N)	Application
VPROC1	MT6365IAW/B MT6365IBW/B	0.75	Y	GPU APU ISP
VPROC2	MT6365IAW/B MT6365IBW/B	0.75	Y	Processor DLA GPU
VGPU11 + VGPU12	MT6365IAW/B MT6365IBW/B	0.75	Y	Processor Digital core always on
VCORE	MT6365IAW/B MT6365IBW/B	0.75	Y	Digital core always on Processor
VMODEM	MT6365IAW/B MT6365IBW/B	0.75	N Y	Processor No used APU
VPU	MT6365IAW/B MT6365IBW/B	0.75 0.75	Y	RF DIG SRAM
LDO name	**Part Number**	**Default voltage (V)**	**Default on (Y/N)**	**Application**
VA09	MT6365IAW/B MT6365IBW/B	0.85 0.85	Y Y N	AP HDMIRX RF
VRFCK	MT6365IAW/B	1.6	Y	MT6365 internal use (DCXO)
VEMC	MT6365IAW/B	3	Y	eMMC and UFS
VSRAM_PROC1	MT6365IAW/B MT6365IBW/B	0.85	Y	SRAM
VSRAM_PROC2	MT6365IAW/B MT6365IBW/B	0.85	Y	SRAM
VSRAM_OTHERS	MT6365IAW/B	0.75	Y	SRAM
VSRAM_MD	MT6365IAW/B	0.75	Y	SRAM

1.6 Pin Assignments and Description

203	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	NC	VRF12	VS2	VSYS_VS2	VSYS_VPA	VPA	VSYS_VPU	VPU	GND_VMODEM	VMODEM	VSYS_VMODEM	VSYS_VPROC2	VPROC2	GND_VPROC2	VSYS_VPROC1	VSYS_VPROC1	A
B	VRF12_S	VA12	VS2	GND_VS2	GND_VPA	VPA	GND_VPU	VPU	GND_VMODEM	VMODEM	VSYS_VMODEM	VSYS_VPROC2	VPROC2	GND_VPROC2	VPROC1	VPROC1	B
C	VCN13	VS2_LDO2	VA09	VSYS_SMPS	VS2_FB	GND_SMPS	VPA_FB	GND_VPU_FB	VPU_FB	GND_VMODEM_FB	VMODEM_FB	GND_VPROC2_FB		VPROC2_FB	GND_VPROC1	GND_VPROC1	C
D	VSRAM_MD	VS2_LDO1	VSRAM_PROC1	VSRAM_others	EXT_PMIC_PG	EXT_PMIC_EN2	EXT_PMIC_EN1	PWRKEY		CHRDETB	PMU_TESTMODE		HOMEKEY	GND_VPROC1_FB	GND_VGPU12	GND_VGPU12	D
E	AU_V18N	VSRAM_PROC2	RESETB			GND	GND	GND	GND	GND	SPI_CLK	SPI_CSN	SPI_MISO		VGPU12	VGPU12	E
F	FLYN		AU_LOLP	AU_LOLN		AUD_NLE_MOSI0	AUD_SYNC_MOSI	GND	GND	GND		SPI_MOSI		VPROC1_FB	VSYS_VGPU12	VSYS_VGPU12	F
G	FLYP	AVSS18_AUD	AU_HPR	AU_REFN		AUD_NLE_MOSI1	AUD_DAT_MISO1	GND	GND	GND		FSOURCE	SRCLKEN_IN1	VGPU11_FB	VSYS_VGPU11	VSYS_VGPU11	G
H		AVDD18_AUD		AU_HPL		AUD_DAT_MISO0	AUD_CLK_MOSI					RTC32K_1V8_0	SRCLKEN_IN0		VGPU11	VGPU11	H
J	AVDD30_AUD	AVSS30_AUD	AU_HSN	AU_HSP		AUD_DAT_MOSI0	AUD_DAT_MISO2				DVSS18_IO	RTC32K_1V8_1	WDTRSTB_IN	GND_VGPU11_FB	GND_VGPU11	GND_VGPU11	J
K	AVDD18_CODEC		HP_EINT	ACCDET		AUD_DAT_MOSI1	AUD_DAT_MOSI2			DVDD18_DIG	DVDD18_IO	SCP_VREQ_VAO		GND_VCORE_FB	GND_VCORE	GND_VCORE	K
L	AU_VIN0_P	AU_VIN0_N	AU_VIN3_N	AU_VIN3_P	AU_MICBIAS0		BATADC_P	AVSS18_AUXADC	CS_P	CS_N	GND_VREF	VREF	VRTC28		VCORE	VCORE	L
M		AU_VIN1_P	AU_VIN2_P	AU_MICBIAS1	AU_MICBIAS2	XO_WCN		AUXADC_VIN1		VIBR	VSYSSNS	BATON	UVLO_VTH	VCORE_FB	VSYS_VCORE	VSYS_VCORE	M
N	AVSS_XO_ISO	AU_VIN1_N	AU_VIN2_N	AVSS_RFCK	AVSS_BBCK			VAUX18	VFE28	VIO28	VCAMIO	VAUD18	VEFUSE		VS1	VS1	N
P	XTAL1	AVSS_XO	VRFCK_1	XO_CEL	VBBCK	XO_EXT	VUSB	VSIM1	VSYS_LDO2	VSYS_LDO1	VM18	VS1_LDO1	VS1_LDO2	VS1_FB	GND_VS1	VSYS_VS1	P
R	AVSS_XO	XTAL2	VXO22	VRFCK	XO_SOC	XO_NFC	VBIF28	VSIM2	VEMC	VCN33_1	VCN33_2	VUFS	VCN18	VRF18	VIO18	NC	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 1-1. MT6365 WFBGA 203 (5.98 x 5.62 mm) pin assignment (top view)

Table 1-3. MT6365 pin description

Ball	Symbol	I/O	Description
N8	VAUX18	O	VAUX18 output voltage
R7	VBIF28	O	VBIF28 output voltage
N9	VFE28	O	VFE28 output voltage
R10	VCN33_1	O	VCN33_1 output voltage
R11	VCN33_2	O	VCN33_2 output voltage
R9	VEMC	O	VEMC33 output voltage
P8	VSIM1	O	VSIM1 output voltage
R8	VSIM2	O	VSIM2 output voltage
M10	VIBR	O	VIBR output voltage
N10	VIO28	O	VIO28 output voltage
P7	VUSB	O	VUSB output voltage
N12	VAUD18	O	VAUD18 output voltage
N11	VCAMIO	O	VCAMIO output voltage
R13	VCN18	O	VCN18 output voltage
N13	VEFUSE	O	VEFUSE output voltage
R15	VIO18	O	VIO18 output voltage
P11	VM18	O	VM18 output voltage
R14	VRF18	O	VRF18 output voltage
R12	VUFS	O	VUFS output voltage
C3	VA09	O	VA09 output voltage
B2	VA12	O	VA12 output voltage
C1	VCN13	O	VCN13 output voltage
A2	VRF12	O	VRF12 output voltage
B1	VRF12_S	I	LDO VRF12 feedback pin

Ball	Symbol	I/O	Description
D3	VSRAM_PROC1	O	VSRAM_PROC1 output voltage
E2	VSRAM_PROC2	O	VSRAM_PROC2 output voltage
D4	VSRAM_OTHERS	O	VSRAM_OTHERS output voltage
D1	VSRAM_MD	O	VSRAM_MD output voltage
P12	VS1_LDO1	PWR	2V power supply of SLDO1
P13	VS1_LDO2	PWR	2V power supply of SLDO1
D2	VS2_LDO1	PWR	1.35V power supply of SLDO2
C2	VS2_LDO2	PWR	1.35V power supply of SLDO2
P10	VSYS_LDO1	PWR	Power supply input of LDO group 1
P9	VSYS_LDO2	PWR	Power supply input of LDO group 2
K4	ACCDET	I	Accessory detection input
H4	AU_HPL	O	Earphone left channel output
G3	AU_HPR	O	Earphone right channel output
J3	AU_HSN	O	Handset negative output
J4	AU_HSP	O	Handset positive output
F4	AU_LOLN	O	Lineout negative output
F3	AU_LOLP	O	Lineout positive output
L5	AU_MICBIAS0	O	Microphone bias 0
M4	AU_MICBIAS1	O	Microphone bias 1
M5	AU_MICBIAS2	O	Microphone bias 2
G4	AU_REFN	GND	Audio reference ground
L2	AU_VIN0_N	I	Microphone channel 0 negative input
L1	AU_VIN0_P	I	Microphone channel 0 positive input
N2	AU_VIN1_N	I	Microphone channel 1 negative input
M2	AU_VIN1_P	I	Microphone channel 1 positive input
N3	AU_VIN2_N	I	Microphone channel 2 negative input
M3	AU_VIN2_P	I	Microphone channel 2 positive input
L3	AU_VIN3_N	I	Microphone channel 3 negative input
L4	AU_VIN3_P	I	Microphone channel 3 positive input
K3	HP_EINT	I	HPL detection
E1	AU_V18N	PWR	Audio -1.8V supply
H2	AVDD18_AUD	PWR	1.8V power supply of audio
K1	AVDD18_CODEC	PWR	1.8V power supply of CODEC
J1	AVDD30_AUD	PWR	Power supply of audio UL
G2	AVSS18_AUD	GND	Audio DL ground
J2	AVSS30_AUD	GND	Audio UL ground
F1	FLYN	O	Flying capacitor bottom
G1	FLYP	O	Flying capacitor top
L7	BATADC_P	I	AUXADC + input pin for monitoring battery voltage
M8	AUXADC_VIN1	I	AUXADC input 1 (GPS CO-CLK)
L8	AVSS18_AUXADC	GND	AUXADC ground
C6	GND_SMPS	GND	GND of buck controller
C4	VSYS_SMPS	PWR	Power supply of buck controller
K15, K16	GND_VCORE	GND	Ground of CORE
K14	GND_VCORE_FB	I	Remote sense on ground of VCORE
L15, L16	VCORE	O	SW node of VCORE
M14	VCORE_FB	I	BUCK VCORE feedback pin on Vout

Ball	Symbol	I/O	Description
M15, M16	VSYS_VCORE	PWR	Power supply of VCORE
A14, B14	GND_VPROC2	GND	Ground of VPROC2
C12	GND_VPROC2_FB	I	Remote sense on ground of VPROC2
A13, B13	VPROC2	O	SW node of VPROC2
C14	VPROC2_FB	I	BUCK VPROC2 feedback pin on Vout
A12, B12	VSYS_VPROC2	PWR	Power supply of VPROC2
B7	GND_VPU	GND	Ground of VPU
C8	GND_VPU_FB	I	Remote sense on ground of VPU
A8, B8	VPU	O	SW node of VPU
C9	VPU_FB	I	BUCK VPU feedback pin on Vout
A7	VSYS_VPU	PWR	Power supply of VPU
A9, B9	GND_VMODEM	GND	Ground of VMODEM
C10	GND_VMODEM_FB	I	Remote sense on ground of VMODEM
A10, B10	VMODEM	O	SW node of VMODEM
C11	VMODEM_FB	I	BUCK VMODEM feedback pin on Vout
A11, B11	VSYS_VMODEM	PWR	Power supply of VMODEM
B5	GND_VPA	GND	Ground of VPA
A6, B6	VPA	O	SW node of VPA
C7	VPA_FB	I	BUCK VPA feedback pin on Vout
A5	VSYS_VPA	PWR	Power supply of VPA
P15	GND_VS1	GND	Ground of VS1
N15, N16	VS1	O	SW node of VS1
P14	VS1_FB	I	BUCK VS1 feedback pin on Vout
P16	VSYS_VS1	PWR	Power supply of VS1
B4	GND_VS2	GND	Ground of VS2
A3, B3	VS2	O	SW node of VS2
C5	VS2_FB	I	BUCK VS2 feedback pin on Vout
A4	VSYS_VS2	PWR	Power supply of VS2
C15, C16	GND_VPROC1	GND	Ground of VPROC1
D14	GND_VPROC1_FB	I	Remote sense on ground of VPROC1
B15, B16	VPROC1	O	SW node of VPROC1
F14	VPROC1_FB	I	BUCK VPROC1 feedback pin on Vout
A15, A16	VSYS_VPROC1	PWR	Power supply of VPROC1
J15, J16	GND_VGPU11	GND	Ground of VGPU11
J14	GND_VGPU11_FB	I	Remote sense on ground of VGPU11
H15, H16	VGPU11	O	SW node of VGPU11
G14	VGPU11_FB	I	BUCK VGPU11 feedback pin on Vout
G15, G16	VSYS_VGPU11	PWR	Power supply of VGPU11
D15, D16	GND_VGPU12	GND	Ground of VGPU12
E15, E16	VGPU12	O	SW node of VGPU12
F15, F16	VSYS_VGPU12	PWR	Power supply of VGPU12
P2, R1	AVSS_XO	GND	Ground for XO
N1	AVSS_XO_ISO	GND	Connect to GSUB for DCXO noise isolation
N4	AVSS_RFCK	GND	Ground for RF clock buffer
N5	AVSS_BBCK	GND	Ground for baseband clock buffer
R3	VXO22	O	VXO22 output voltage
R4	VRFCK	O	RF clock buffer power source

Ball	Symbol	I/O	Description
P3	VRFCK_1	O	RF clock buffer power source
P5	VBBCK	O	Baseband clock buffer power source
P4	XO_CEL	O	RF clock buffer output to Cell. RF
P6	XO_EXT	O	Baseband clock buffer output to UFS
R6	XO_NFC	O	Baseband clock buffer output to NFC
R5	XO_SOC	O	Baseband clock buffer output to SOC
M6	XO_WCN	O	RF clock buffer output to Conn. RF
P1	XTAL1	I	XTAL input
R2	XTAL2	O	XTAL output
F6	AUD_NLE_MOSI0	I	Audio control interface
H7	AUD_CLK_MOSI	I	Audio control interface
H6	AUD_DAT_MISO0	O	Audio control interface
G7	AUD_DAT_MISO1	O	Audio control interface
J7	AUD_DAT_MISO2	O	Audio control interface
J6	AUD_DAT_MOSI0	I	Audio control interface
K6	AUD_DAT_MOSI1	I	Audio control interface
K7	AUD_DAT_MOSI2	I	Audio control interface
G6	AUD_NLE_MOSI1	I	Audio control interface
F7	AUD_SYNC_MOSI	I	Audio control interface
K10	DVDD18_DIG	PWR	VDIG18 output voltage
K11	DVDD18_IO	PWR	Digital IO power
J11	DVSS18_IO	GND	Digital IO power GND
G12	FSOURCE	PWR	EFUSE power source
H12	RTC32K_1V8_0	O	VIO18 domain 32 kHz clock output
J12	RTC32K_1V8_1	O	VIO18 domain 32 kHz clock output
E11	SPI_CLK	I	SPI control interface
E12	SPI_CSN	I/O	SPI control interface
E13	SPI_MISO	I/O	SPI control interface
F12	SPI_MOSI	I/O	SPI control interface
H13	SRCLKEN_IN0	I	Source clock enable pin 0
G13	SRCLKEN_IN1	I	Source clock enable pin 1
K12	SCP_VREQ_VAO	I	Voltage source request input pin, connected to SOC
D13	HOMEKEY	I	HOMEKEY button
J13	WDTRSTB_IN	I	Watchdog reset from AP
L10	CS_N	I	Fuel gauge ADC input pin
L9	CS_P	I	Fuel gauge ADC input pin
D7	EXT_PMIC_EN1	O	Ext PMIC enable pin 1
D6	EXT_PMIC_EN2	O	Ext PMIC enable pin 2
D5	EXT_PMIC_PG	I	Ext PMIC power-good pin
D10	CHRDETB	I	Charger detection signal from sub PMIC
D11	PMU_TESTMODE	I	PMU test mode signal (tied to GND in normal operation)
D8	PWRKEY	I	PWRKEY button
E3	RESETB	O	System reset release signal
M12	BATON	I	Battery NTC pin for battery and its temperature sensing
L11	GND_VREF	GND	Ground for bandgap

Ball	Symbol	I/O	Description
M13	UVLO_VTH	I	UVLO threshold control pin
L12	VREF	O	Bandgap reference voltage
M11	VSYSSNS	I	VSYS supply input for internal block and UVLO detection
L13	VRTC28	O	RTC LDO output. Supply of RTC macro where backup battery can be added.
E6, E7, E8, E9, E10, F8, F9, F10, G8, G9, G10	D_GND	GND	Ground
A1, R16	DUMMY	NC	NC

2 Electrical Characteristics

2.1 Absolute Maximum Ratings over Operating Free-Air Temperature Range

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device. These numbers are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 2-1. Absolute maximum ratings

Parameter	Condition	Min.	Typ.	Max.	Unit
Free-air temperature range		-40		85	°C
Storage temperature range		-65		150	°C
Battery pin input (1)	Steady state	-0.5		6	V
	Transient (< 10 ms)	-0.5		7	V
Non-battery power pin (2)	Steady state	-0.5		5	V
Signal pins (3)	Steady state	-0.5		Vxx+0.5(3)	V
ESD robustness	HBM	2,000			V

(1) Note 1 VSYS_XXX/Vxxx (BUCK SW node)/VSYSSNS/BATADC -> battery input pin

(2) Note 2 Non-battery power input -> reference Table 2-1 (PWR pin but not connected with battery)

(3) Note 3 Vxx = Max. operation voltage (refer to Table 2-2)

2.2 Thermal Characteristics

Table 2-2. Thermal characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Thermal resistance from junction to ambient	In free air		40.5		°C/W

Note. The device is mounted on an 8-metal-layer PCB and modeled per JEDEC51-9 condition.

2.3 Pin Voltage Range

The table below lists the operation rang voltages for all MT6365 I/O pins.

Table 2-3. Pin voltage range

Ball	Symbol	Voltage range	Unit
N8	VAUX18	0 ~ 1.98	V
R7	VBIF28	0 ~ 5	V
N9	VFE28	0 ~ 5	V
R10	VCN33_1	0 ~ 5	V
R11	VCN33_2	0 ~ 5	V

Ball	Symbol	Voltage range	Unit
R9	VEMC	0 ~ 5	V
P8	VSIM1	0 ~ 5	V
R8	VSIM2	0 ~ 5	V
M10	VIBR	0 ~ 5	V
N10	VIO28	0 ~ 5	V
P7	VUSB	0 ~ 5	V
N12	VAUD18	0 ~ 2.2	V
N11	VCAMIO	0 ~ 2.2	V
R13	VCN18	0 ~ 2.2	V
N13	VEFUSE	0 ~ 2.2	V
R15	VIO18	0 ~ 2.2	V
P11	VM18	0 ~ 2.2	V
R14	VRF18	0 ~ 2.2	V
R12	VUFS	0 ~ 2.2	V
C3	VA09	0 ~ 2.2	V
B2	VA12	0 ~ 2.2	V
C1	VCN13	0 ~ 2.2	V
A2	VRF12	0 ~ 2.2	V
B1	VRF12_S	0 ~ 2.2	V
D3	VSRAM_PROC1	0 ~ 1.4	V
E2	VSRAM_PROC2	0 ~ 1.4	V
D4	VSRAM_OTHERS	0 ~ 1.4	V
D1	VSRAM_MD	0 ~ 1.4	V
P12	VS1_LDO1	0 ~ 2.2	V
P13	VS1_LDO2	0 ~ 2.2	V
D2	VS2_LDO1	0 ~ 2.2	V
C2	VS2_LDO2	0 ~ 2.2	V
P10	VSYS_LDO1	0 ~ 5	V
P9	VSYS_LDO2	0 ~ 5	V
K4	ACCDET	0 ~ 3.3	V
H4	AU_HPL	-2.1 ~ +2.1	V
G3	AU_HPR	-2.1 ~ +2.1	V
J3	AU_HSN	-2.1 ~ +2.1	V
J4	AU_HSP	-2.1 ~ +2.1	V
F4	AU_LOLN	-2.1 ~ +2.1	V
F3	AU_LOLP	-2.1 ~ +2.1	V
L5	AU_MICBIAS0	0 ~ 3.3	V
M4	AU_MICBIAS1	0 ~ 3.3	V
M5	AU_MICBIAS2	0 ~ 3.3	V
G4	AU_REFN	0	V
L2	AU_VIN0_N	0 ~ 3.3	V
L1	AU_VIN0_P	0 ~ 3.3	V
N2	AU_VIN1_N	0 ~ 3.3	V
M2	AU_VIN1_P	0 ~ 3.3	V
N3	AU_VIN2_N	0 ~ 3.3	V
M3	AU_VIN2_P	0 ~ 3.3	V
L3	AU_VIN3_N	0 ~ 3.3	V

Ball	Symbol	Voltage range	Unit
L4	AU_VIN3_P	0 ~ 3.3	V
K3	HP_EINT	-2.1 ~ 3.3	V
E1	AU_V18N	-2.1 ~ 0	V
H2	AVDD18_AUD	0 ~ 2.1	V
K1	AVDD18_CODEC	0 ~ 1.98	V
J1	AVDD30_AUD	0 ~ 3.3	V
G2	AVSS18_AUD	0	V
J2	AVSS30_AUD	0	V
F1	FLYN	-2.1 ~ 0	V
G1	FLYP	0 ~ 2.1	V
L7	BATADC_P	0 ~ 5	V
M8	AUXADC_VIN1	0 ~ 1.84	V
L8	AVSS18_AUXADC	0	V
C6	GND_SMPS	0	V
C4	VSYS_SMPS	0 ~ 5	V
K15, K16	GND_VCORE	0	V
K14	GND_VCORE_FB	0	V
L15, L16	VCORE	0 ~ 5	V
M14	VCORE_FB	0 ~ 5	V
M15, M16	VSYS_VCORE	0 ~ 5	V
A14, B14	GND_VPROC2	0	V
C12	GND_VPROC2_FB	0	V
A13, B13	VPROC2	0 ~ 5	V
C14	VPROC2_FB	0 ~ 5	V
A12, B12	VSYS_VPROC2	0 ~ 5	V
B7	GND_VPU	0	V
C8	GND_VPU_FB	0	V
A8, B8	VPU	0 ~ 5	V
C9	VPU_FB	0 ~ 5	V
A7	VSYS_VPU	0 ~ 5	V
A9, B9	GND_VMODEM	0	V
C10	GND_VMODEM_FB	0	V
A10, B10	VMODEM	0 ~ 5	V
C11	VMODEM_FB	0 ~ 5	V
A11, B11	VSYS_VMODEM	0 ~ 5	V
B5	GND_VPA	0	V
A6, B6	VPA	0 ~ 5	V
C7	VPA_FB	0 ~ 5	V
A5	VSYS_VPA	0 ~ 5	V
P15	GND_VS1	0	V
N15, N16	VS1	0 ~ 5	V
P14	VS1_FB	0 ~ 5	V
P16	VSYS_VS1	0 ~ 5	V
B4	GND_VS2	0	V
A3, B3	VS2	0 ~ 5	V
C5	VS2_FB	0 ~ 5	V
A4	VSYS_VS2	0 ~ 5	V

Ball	Symbol	Voltage range	Unit
C15, C16	GND_VPROC1	0	V
D14	GND_VPROC1_FB	0	V
B15, B16	VPROC1	0 ~ 5	V
F14	VPROC1_FB	0 ~ 5	V
A15, A16	VSYS_VPROC1	0 ~ 5	V
J15, J16	GND_VGPU11	0	V
J14	GND_VGPU11_FB	0	V
H15, H16	VGPU11	0 ~ 5	V
G14	VGPU11_FB	0 ~ 5	V
G15, G16	VSYS_VGPU11	0 ~ 5	V
D15, D16	GND_VGPU12	0	V
E15, E16	VGPU12	0 ~ 5	V
F15, F16	VSYS_VGPU12	0 ~ 5	V
P2, R1	AVSS_XO	0	V
N1	AVSS_XO_ISO	0	V
N4	AVSS_RFCK	0	V
N5	AVSS_BBCK	0	V
R3	VXO22	0 ~ 2.42	V
R4	VRFCK	0 ~ 1.76	V
P3	VRFCK_1	0 ~ 1.76	V
P5	VBBCK	0 ~ 1.32	V
P4	XO_CEL	0 ~ 1.76	V
P6	XO_EXT	0 ~ 1.32	V
R6	XO_NFC	0 ~ 1.32	V
R5	XO_SOC	0 ~ 1.32	V
M6	XO_WCN	0 ~ 1.76	V
P1	XTAL1	-0.2 ~ 2.2	V
R2	XTAL2	0.2 ~ 1.7	V
F6	AUD_NLE_MOSI0	0 ~ 1.98	V
H7	AUD_CLK_MOSI	0 ~ 1.98	V
H6	AUD_DAT_MISO0	0 ~ 1.98	V
G7	AUD_DAT_MISO1	0 ~ 1.98	V
J7	AUD_DAT_MISO2	0 ~ 1.98	V
J6	AUD_DAT_MOSI0	0 ~ 1.98	V
K6	AUD_DAT_MOSI1	0 ~ 1.98	V
K7	AUD_DAT_MOSI2	0 ~ 1.98	V
G6	AUD_NLE_MOSI1	0 ~ 1.98	V
F7	AUD_SYNC_MOSI	0 ~ 1.98	V
K10	DVDD18_DIG	0 ~ 1.98	V
K11	DVDD18_IO	0 ~ 1.98	V
J11	DVSS18_IO	0	V
G12	FSOURCE	0 ~ 1.98	V
H12	RTC32K_1V8_0	0 ~ 1.98	V
J12	RTC32K_1V8_1	0 ~ 1.98	V
E11	SPI_CLK	0 ~ 1.98	V
E12	SPI_CSN	0 ~ 1.98	V
E13	SPI_MISO	0 ~ 1.98	V

Ball	Symbol	Voltage range	Unit
F12	SPI_MOSI	0 ~ 1.98	V
H13	SRCLKEN_IN0	0 ~ 1.98	V
G13	SRCLKEN_IN1	0 ~ 1.98	V
K12	SCP_VREQ_VAO	0 ~ 1.98	V
D13	HOMEKEY	0 ~ 1.98	V
J13	WDTRSTB_IN	0 ~ 1.98	V
L10	CS_N	-0.1 ~ 1.8	V
L9	CS_P	-0.1 ~ 1.8	V
D7	EXT_PMIC_EN1	0 ~ 5	V
D6	EXT_PMIC_EN2	0 ~ 5	V
D5	EXT_PMIC_PG	0 ~ 5	V
D10	CHRDETB	0 ~ 5	V
D11	PMU_TESTMODE	0 ~ 5	V
D8	PWRKEY	0 ~ 5	V
E3	RESETB	0 ~ 1.98	V
M12	BATON	0 ~ 3.08	V
L11	GND_VREF	0	V
M13	UVLO_VTH	0 ~ 3.3	V
L12	VREF	0 ~ 1.32	V
M11	VSYSSNS	0 ~ 5	V
L13	VRTC28	0 ~ 2.98	V
E6, E7, E8, E9, E10, F8, F9, F10, G8, G9, G10	D_GND	0	V
A1, R16	DUMMY	NC	V

2.4 Recommended Operating Range

Table 2-4. Operation condition

Parameter	Condition	Min.	Typ.	Max.	Unit
Ambient temperature (TA)		-40		85	°C
Junction temperature (TJ)		-40		125	°C
Operating input voltage		3.15 (1)		5	V

(1) Note 1 This minimum input voltage still needs to check the detailed test conditions for each function in specification table.

2.5 Electrical Characteristics

- VBAT = 2.6~5V, minimum loads applied on all outputs, unless otherwise noted.
- Typical values are at TA = 25°C.

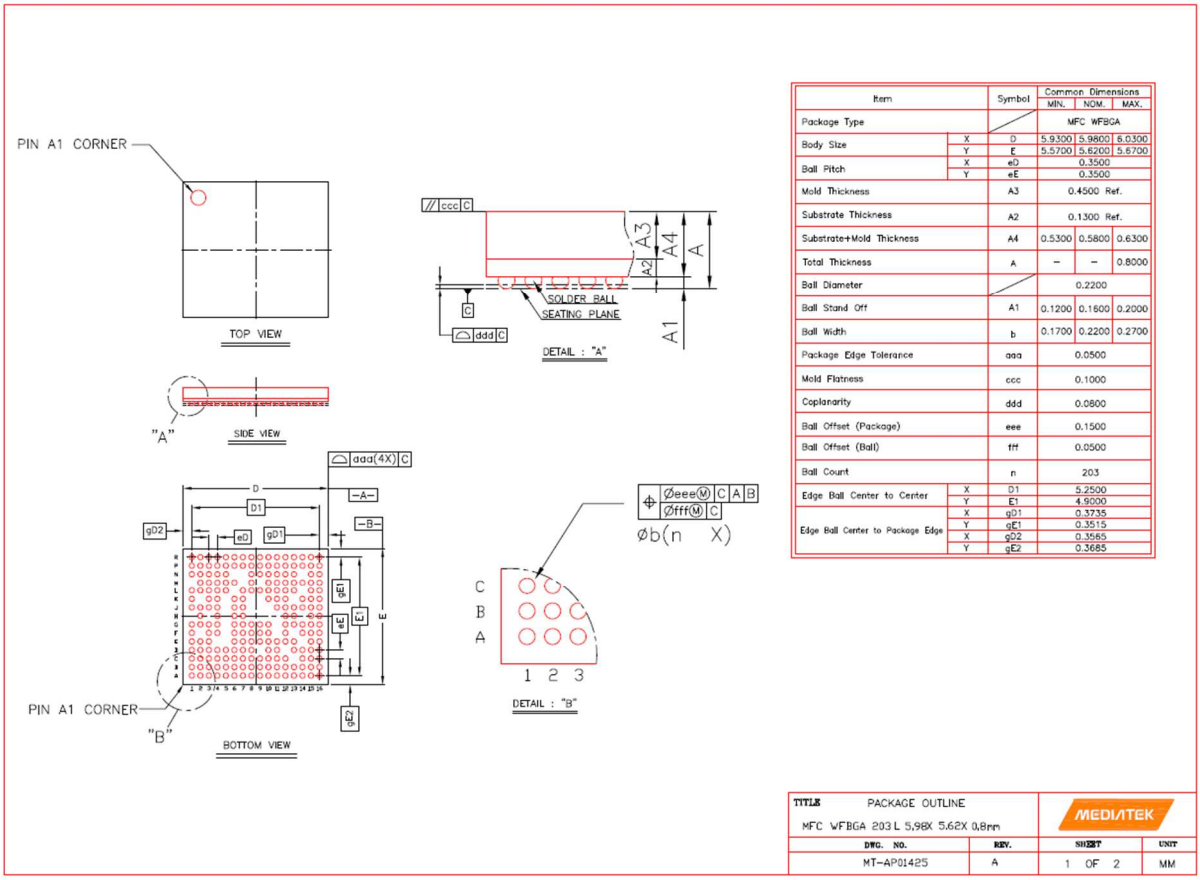
Table 2-5. General electrical specification

Parameter	Condition	Min.	Typ.	Max.	Unit
Operation Ground Current					
Standby without 32K XTAL	VBAT = 4V, low-power mode		510	665	µA

Power down leakage current without 32K XTAL	VBAT = 4V Temp = 25°C			85	uA
Under Voltage Lock-Out (UVLO)					
Under voltage falling threshold		2.55	2.6	2.65	V
Under voltage rising threshold	R = 200K	2.95	3.0	3.05	V
Over Voltage Lock-Out (OVLO)					
Over voltage falling threshold		5.1	5.2	5.3	V
Over voltage rising threshold		5.5	5.6	5.7	V
Reset Generator					
Output high		VIO - 0.4			V
Output low				0.2	V
PWRKEY					
High voltage		1.45			V
Low voltage				0.3	V
De-bounce time			32		ms
Control Input Voltage					
Control input high (SPI, SRCLKEN related)		0.75*VIO			V
Control input low (SPI, SRCLKEN related)				0.25*VIO	V
Thermal Shut-Down					
PMIC shut-down threshold			150		°C
Shut-down release threshold			110		°C

3 MT6365 Packaging

3.1 Package Dimensions



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			MFC WFBGA		
Body Size	X	D	5.9300	5.9800	6.0300
	Y	E	5.5700	5.6200	5.6700
Ball Pitch	X	eD	0.3500		
	Y	eE	0.3500		
Mold Thickness		A3	0.4500 Ref.		
Substrate Thickness		A2	0.1300 Ref.		
Substrate+Mold Thickness		A4	0.5300	0.5800	0.6300
Total Thickness		A	–	–	0.8000
Ball Diameter			0.2200		
Ball Stand Off		A1	0.1200	0.1600	0.2000
Ball Width		b	0.1700	0.2200	0.2700
Package Edge Tolerance		aaa	0.0500		
Mold Flatness		ccc	0.1000		
Coplanarity		ddd	0.0800		
Ball Offset (Package)		eee	0.1500		
Ball Offset (Ball)		fff	0.0500		
Ball Count		n	203		
Edge Ball Center to Center	X	D1	5.2500		
	Y	E1	4.9000		
Edge Ball Center to Package Edge	X	gD1	0.3735		
	Y	gE1	0.3515		
	X	gD2	0.3565		
	Y	gE2	0.3685		

TITLE	PACKAGE OUTLINE MFC WFBGA 203 L 5.98X 5.62X 0.8mm		
DWG. NO.	REV.	SHEET	UNIT
MT-AP01425	A	1 OF 2	MM

Figure 3-1. Package dimensions

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